UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/082,144	02/25/2002	Victor Roberts Augsburg	RPS920010176US1	2686

			EXAMINER
45211	7590	01/13/2005	COLEMAN, ERIC

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ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 01/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO 90C (Rev 10/03)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _18 October 2004_.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-51_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1,5,8,16,19,27,30,38,41 and 49_ is/are rejected.

7)☒ Claim(s) _2-4,6,7,9-15,17,18,20-26,28,29,31-37,39,40,42-48,50 and 51_ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some *   c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2.   Claims 1,5,8,16,19,27,30,38,41,49 are rejected under 35 U.S.C. 102(b) as being

anticipated by Witt (patent No. 6,167,506).

3.   Witt taught (claims 1,8,19,30,41) the invention as claimed including a data

processing ("DP") system comprising: fetching a branch instruction from memory,

wherein the branch instruction stores an offset of a target address comprising n bits;

calculating n-1 least significant bits of the target address of the branch instruction; and

replacing n-1 least significant bits of the target address of the branch instruction (e.g.,

see figs. 2,4,4a; col. 3, line 64-col. 4, line 37; col. 21, lines 13-40; and col. 23, lines 3-

63).

4.   As to further limitations of claims 8,19,30 (the instruction memory and cache) Witt

taught instruction queue (20) and instruction memory (80) caches (14,16,38) and main

memory 204) (e.g., see figs. 1,15) and encoder (106) (e.g., see fig.4a) and col. 21, lines

13-48).

5.   As per claims (5,16,27,38,49) Witt taught the calculating comprising adding a

value stored the value in the least significant bits of the offset of the target address

stored in the branch instruction with a value stored in the n-1 least significant bits of the

address of the branch instruction (e.g., see col. 22, lines 4-30).

Response to Arguments

6.   The rejections of claims 1, 5, 8, 16, 19, 27, 30, 38, 41, 49 are maintained as set

forth in the last office action (and repeated above).

7.   Applicant's arguments filed 10/29/04 have been fully considered but they are not

persuasive.

8.   In the remarks, the applicant argues in substance that:

        a) Witt did not teach Calculating n-1 least significant bits of the target address of

the branch instruction. As to this allegation the Examiner contends that Witt taught

calculation of the target address of the branch instruction as described in the rejection

above. Also in order for the target address to be calculated each of the least significant

bits (which includes any arbitrary n-1 grouping of the least significant bits) would have

been required to be calculated. Otherwise the address would have been incomplete for

use in providing a target address for branching.

        b) Witt did not teach replacing n-1 least significant bits of an offset of a said

target address with n-1 least significant bits of said target address of the branch

instruction. As to this allegation the Examiner contends Witt taught replacing the branch

displacement, which is the offset of the target address, with the calculated address by

adding the entire branch address with the displacement as indicated in the rejection

above. In order to add the displacement with the branch address, the corresponding bits of the displacement would have been required to have been added to the corresponding bits of the branch address. Therefore the least significant bits of the displacement would have to have been added to the least significant bits of the branch address to generate the target address. Consequently the calculated target address would have had least significant bits that consisted of the bits branch address that were increased by the amount of the addition of the value of the displacement without the change of the most significant bits of the branch address. Witt taught replacing the displacement in the instruction with the calculated branch target and therefore the least significant bits would have been required to be replaced by the corresponding bits of the calculated target address. This would have included any arbitrary n-1 grouping of least significant bits.

c) As per claims 5,16,27,38 and 49 Witt did not teach adding a value stored in the n-1 least significant bits of an offset of a target address stored in the branch instruction with a value stored in said n-1 least significant bits of said address of said branch instruction. As to this allegation the Examiner contends Witt taught adding the stored displacement of a target address stored in a branch instruction with a value stored in the address of the branch instruction to calculate the address of the target as indicated in the rejection above. The Examiner contends in order to perform the calculation of the target Witt would have been required to add each corresponding bit of the displacement to each corresponding bit of the branch address. This would have included any arbitrary grouping of n-1 least significant bits.

Allowable Subject Matter

9.   Claims 2-4,6-7,9-15,17-18,20-26,28,29,31-37,39,40,42-48,50, and 51 are

objected to as being dependent upon a rejected base claim, but would be allowable if

rewritten in independent form including all of the limitations of the base claim and any

intervening claims.

Conclusion

10.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Eric Coleman whose telephone number is (571) 272-

4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for

the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

EC

ERIC COLEMAN
PRIMARY EXAMINER